ABSTRACT

The semiconductor testing apparatus includes test pattern memory means adapted for storing and managing test pattern data in accordance with addresses, and outputting the test pattern specified by the desired address; test pattern generation means for generating a test pattern signal on the basis of the test pattern outputted from the memory means; and control means for controlling the test pattern memory means and the test pattern generation means in such a manner that the test pattern signal based on the test pattern data of the desired address can be generated at a predetermined timing conforming with the set information.